

HM15195 High Efficiency DC/DC Module

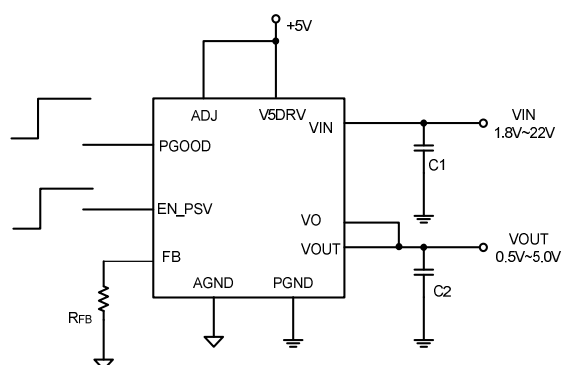
FEATURES

- Complete Switch Mode Power Supply
- Wide Input Voltage Range from +1.8V to 22V
- 15A DC Output Current
- Adjustable +0.5V to + 5V Output Range
- Fast Transient Response
- Power Saving Mode Option
- Enable Function Option
- Power Good Indicator
- Internal Soft-Start
- Whole Protection Functions
- Pb-Free RoHS Compliant Package
- Small Footprint, Low Profile Surface Mount Hybrid Package (11mm*12mm*1.8mm)
Choke Dimension (11mm*11mm*4.2mm)

APPLICATIONS

- Note Book Computers, UMPC
- I/O Supplies
- System Power Supplier
- Point of Load

TYPICAL SCHEMATIC



DESCRIPTION

The HM15195 is a complete 15A, DC/DC step down power supply. Included in the package have the PWM controller, power MOSFETs, inductor, and most of support components. Operating over an input voltage range of 1.8V to 22V and supports an output voltage range of 0.5V to 5V that set by single dividing resistor. The high efficiency design delivers 15A continuous current. Only bulk input, output capacitors and few parameter setting components are needed to finish the design.

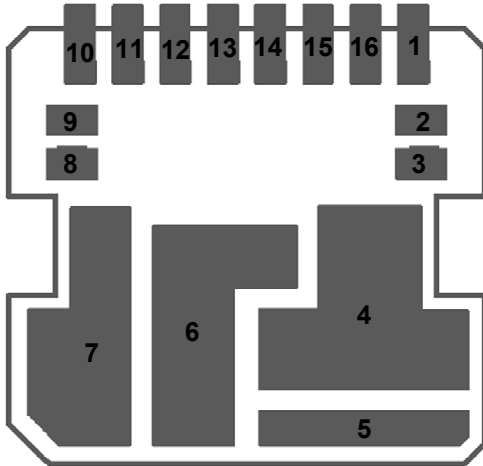
The HM15195 uses constant on-time control for fast transient response. The HM15195 has internal soft-start, current limit, over voltage protection, under voltage protection, power good output and soft discharge upon shutdown. The HM15195 can be configured to operate power saving mode (PSV) or not. At light loads, PSV enables the PWM controller to skip PWM pulses for better efficiency. The HM15195 has been set initial frequency and current limit for normally application which easy to design for power converter.

The low profile package enables utilization of unused space on the bottom of PC boards for highly density point of load regulation. The HM15195 is packaged in a thermally enhanced, compact (11mm×12mm) and low profile (6.2mm) over-molded Hybrid Package Modular suitable for automated assembly by standard surface mount equipment. The HM15195 is Pb-free and RoHS compliance.

MODULE INFORMATION

Bottom View

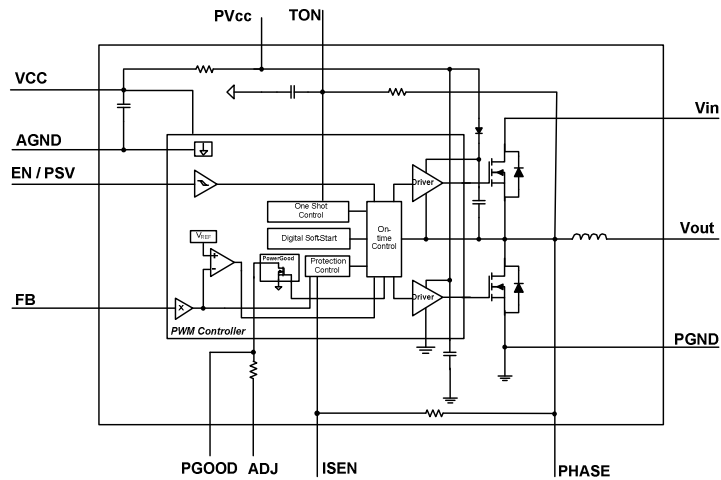
Physical View



Pin Definition:

Pin	Name	Description
1	VCC	5V power supply to PWM controller except gate drivers. Apply RC filter at this pin input. The RC filter is an option. User has no need to install.
2	PGND	Power Ground
3	PVCC	5V power supply for gate drivers. Connect 1uF or more between this pin and PGND to support instantaneous current for gate drivers. This capacitor is an optional component. User has no need to install.
4	PHASE	High side MOSFET gate driver return
5	PGND	Power ground
6	VIN	Connect to Input
7	VOOUT	Connect to output
8	ISEN	Setting over-current protection point. Connect resistor from this pin to PHASE to setting over-current threshold. User has no need to install, a 20kOhm is integrated.
9	EN_PSV	Enable/Power save pin. Connect to ground to disable module. Connect to 3.3V or 5V to turn on module and activate power save mode. Float to turn on force CCM.
10	N.C	No need to connect
11	AGND	Analog Ground
12	TON	On Time/Frequency adjustment. Connect to VIN. This resistor is an optional component, so it has not need to install. (1M resistor is integrated)
13	VO	Connect to output for output discharge when module turned off.
14	VFB	Output voltage feedback input. Connect the resistor divider to adjust output.
15	PGOOD	Power-good signal output. No need a pull-up resistor.
16	ADJ	A pull-high resistor 10kOhm is integrated between ADJ pin and PGOOD pin. The pin need to connect with power supply (5V or 3.3V...etc).

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Limits	Unit
TON to AGND	-0.3 to +25	V
PVCC , EN / PSV, FB, PGOOD, Vo, ISEN to AGND	-0.3 to +6	V
PHASE to PGND	-1.2 to +30	V
Tc	100	°C
Tstg	-40 to +125	°C
VIN to PHASE	-1.2 to +30	V
PGND to AGND	-0.3 to +0.3	V

CAUTION : Stress over “Absolute Maximum Ratings” may cause permanent damage.

RECOMMENDED OPERATING RATINGS

Symbol	Parameter	Limits	Unit
VIN	Input supply voltage	1.8 to 22	V
VOUT	Output voltage	0.5 to 5.0	V
Ta	Ambient temperature range	-40 to 85	°C

Note: Over operating free-air temperature range.

ORDER INFORMATION

PART NUMBER	PACKAGE
HM15195	Hybrid Package (11mm × 12mm × 1.8mm)

THERMAL RESISTANCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Rth(j-a)	Thermal resistance from junction to ambient	Note 1	-		-	°C/W

Note 1 : Rth(j-a) is measured with the component mounted on a highly effective thermal conductivity test board on 0 LFM condition. The test board size is 114.3mm*101.5mm*1.6mm with 4 copper layers, and each copper trace thickness is 1 oz. The test condition is complied with JEDECE EIJ/JESD 51 Standards.

ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range, Vin = 12V, Vout = 3.3V/5V, RTON=1MOhm

Input Capacitance=110uF, Output Capacitance=400uF, (Cyntec's EVM)

Input Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{Q(VIN)}	Input supply bias current	I _{out} = 0A V _{out} = 3.3V, Vin = 12V, EN/PSV = 5V Vin = 12V, EN/PSV = Tri-stated V _{out} = 5.0V Vin = 12V, EN/PSV = 5V Vin = 12V, EN/PSV = Tri-stated		60		mA
I _{S(VIN)}	Input supply current	I _{out} = 15A, V _{out} = 5.0V, Vin = 12V		6.91		A
I _{Q(PVCC)}	5V supply bias current	Vin=12V, Vout=5V, I _{out} =0A		12		mA
Output Characteristics						
I _{OUT(DC)}	Load Rating		0	-	15	A
ΔV _{OUT} /ΔV _{IN}	Line regulation accuracy	EN/PSV = Tri-stated, Vin = 3.3V to 22V V _{out} = 3.3V, I _{out} = 0A V _{out} = 3.3V, I _{out} = 15A		0.1		%
ΔV _{OUT} /ΔI _{OUT}	Load regulation accuracy	EN/PSV = Tri-stated I _{out} = 0A to 15A V _{out} = 5.0V, Vin = 12V,		1		%
V _{OUT(AC)}	Output ripple voltage*	EN/PSV = Tri-stated, I _{out} = 15A V _{out} = 5V, Vin = 12V		100		mVp-p

*Note: Output ripple voltage is dependent on ESR of output capacitors. For design of output capacitor ESR, please refer to HM15195 application note.

ELECTRICAL CHARACTERISTICS (CONTINUED)

 Over operating free-air temperature range, $V_{in} = 12V$, $V_{out} = 3.3V/5V$, $R_{TON} = 1M\Omega$

Input Capacitance = 110uF , Output Capacitance = 400uF (Cyntec's EVM)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Dynamic Characteristics						
ΔV_{OUT-DP}	Voltage change for positive load step	IOUT = 10% to 90% of 15A. Current slew rate = 2.5A/uS $V_{in} = 12V$, $V_{out} = 3.3V$ $V_{in} = 12V$, $V_{out} = 5.0V$	-	120	-	mVp-p
ΔV_{OUT-DN}	Voltage change for negative load step	IOUT = 90% to 10% of 15A. Current slew rate = 2.5A/uS $V_{in} = 12V$, $V_{out} = 3.3V$ $V_{in} = 12V$, $V_{out} = 5.0V$	-	120	-	mVp-p
Control Stage						
V_{FBTHR}	FB turn-on threshold	PVCC = 4.5V to 5.5V	0.494	0.5	0.506	V
R_{FB}	Internal resistor between Vo and FB pins			10		k Ω
R_{TONI}	Internal resistor between Vin and TON pins		0.99	1	1.01	M Ω
TON	PWM on-time	$V_{in} = 12V$, $V_{out} = 3.3V$, $I_{out} = 15A$ $R_{TONI} = 1M\Omega$ (Intregated)		850		nS
Vo	Output voltage range		-	0.5	PVCC	V
V_{ENLTHR}	EN low threshold voltage	EN/PSV low	-	1.2		V
V_{ENHTHR}	EN high threshold voltage	EN/PSV high	-	3.1		V
Fault Protection						
R_{SENI}	Internal resistor between ISEN and PHASE pins			20		k Ω
V_{UVF}	Output under voltage fault		-20	-10	-5	%
V_{OVF}	Output over voltage fault		+15	+20	+40	%
$PVCC_{UVTHR}$	PVCC under voltage threshold		3.7	4.0	4.3	V
TP_{OTPL}	Over temperature lockout		-	165	-	$^{\circ}C$
PGOOD Stage						
V_{PGDLV}	PGOOD low output voltage	Sink 1mA	-	-	0.4	V
$V_{PGDUVTHR}$	PGOOD under voltage threshold		-12	-10	-8	%
R_{PGD}	Pull-up resistor			10		k Ω

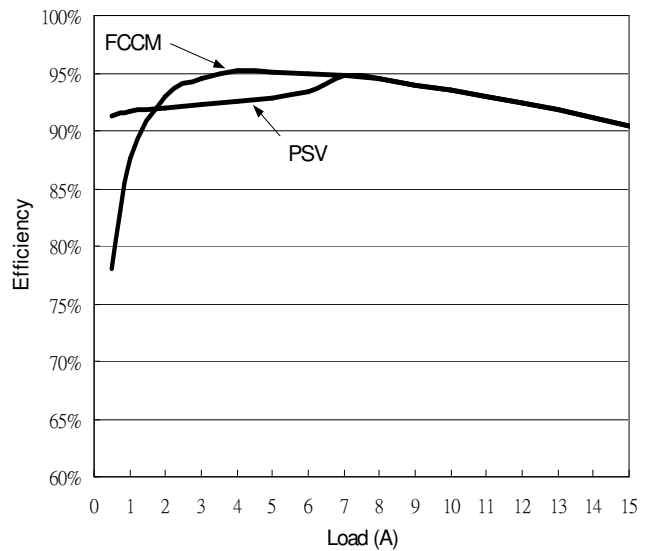
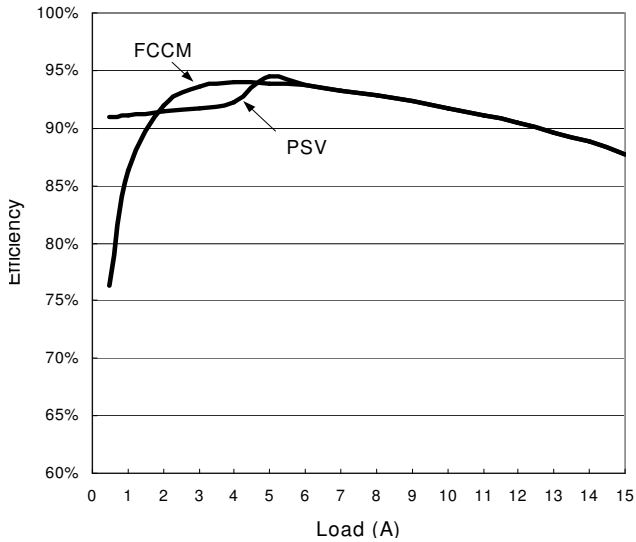
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency Performance : Including Force CCM and Power Save Mode (PSV)

Test Condition: Room Temp., Input Capacitance=110uF, Output Capacitance=400uF (Cyntec's EVM)

VIN=12V/VOUT=3.3V

VIN=12V/VOUT=5.0V

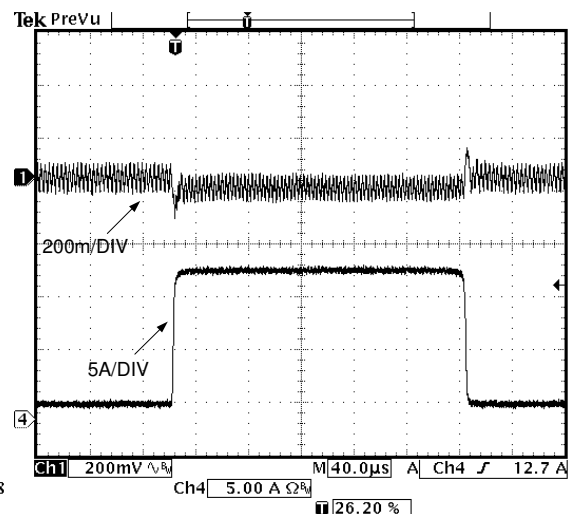
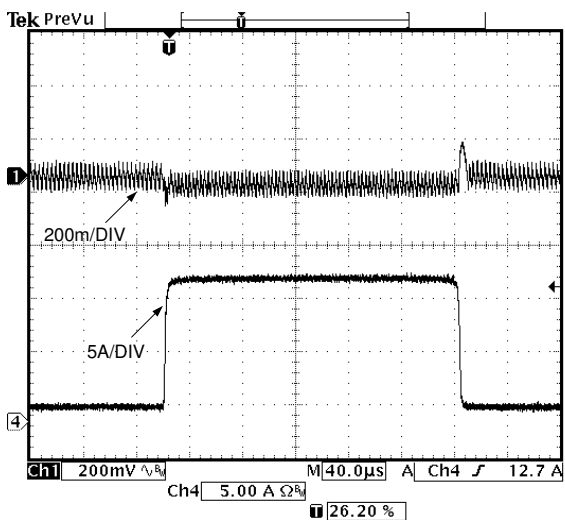


Load Transient Response Performance

Test Condition: Room Temp., Input Capacitance=241uF, Output Capacitance=356uF (Cyntec's EVM), Slew Rate=2.15A/us, Force Continuous Current Mode

Input Voltage=12V, Output Voltage=3.3V

Input Voltage=12V, Output Voltage=5.0V



TYPICAL APPLICATION CIRCUIT:

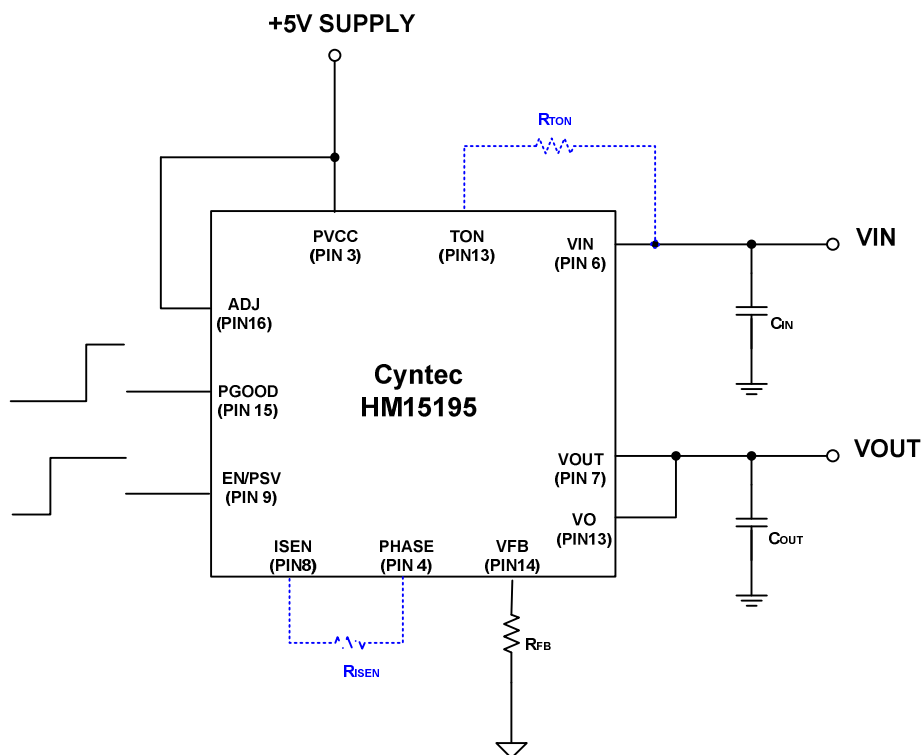


Fig. 1 Reference Circuit

Note: The blue dash lines represent these are options, user has no need to install.

PIN FUNCTIONS

VCC PIN-1

Supply voltage input for internal IC circuits except gate drivers. It can connect a capacitors to enhance filtering capability, but not necessary.

PGND PIN-2, 5

Power ground pin for both input and output return path. It needs to connect one (or more) ground plan immediately which is recommended to minimize the effect of switching noise and copper losses, and maximize heat dissipation.

PVCC PIN-3

The PVCC pin is the supply voltage for gate drivers. This +5V bias supply can be generated by linear or series pass regulator.

PHASE PIN-4

The PHASE pin is the switching node between high and low side MOSFET. It also returns the current path for the high side MOSFET driver. And detecting the low-side MOSFET drain voltage for the over current limits point. Besides, for good thermal performance, the node needs wide but "smart".

VIN PIN-6

Power input pin. Apply input voltage between the pin and PGND pin. Recommend placing input capacitors directly between VIN pin and PGND pin. Besides, the input capacitors should place to module as close as possible.

VOUT PIN-7

Power output pin. Apply output load between the pin and PGND. Recommend placing high frequency output decoupling capacitor between the pin and PGND as close as possible.

ISEN PIN-8

The ISEN pin is the input for the over current protection (OCP) setting. Which compares $R_{ds(on)}$ of low-side MOSFET to set the threshold. The HM15195 has an initial threshold which is about 20A. Hence, user does not need to design the threshold if the threshold meets user's requirement. About the threshold setting, can refer to application note of HM15195. Beside, it also can connect additional resistor between PHASE pin and ISEN pin to decrease the threshold.

EN_PSV PIN-9

The EN / PSV pin enables the supply. When EN / PSV is tied to PVCC, the HM15195 is enabled and power save will able be enabled. When the EN / PSV pin is tri-stated, an internal pull-up will activate the HM15195 and power save will be disabled.

N.C PIN-10

AGND PIN-11

The pin is the common of the HM15195. All signals should be referenced to the pin, NOT the PGND pin. Note: signals like feedback signal of output, feedback pin signal...etc.

PIN FUNCTIONS (CONTINUED)

TON PIN-12

The TON pin programs the PWM switching frequency due to it can determine the high-side switch turn-on time. The HM15195 has initial set this parameter to approach integrated completely. It is included internal 1M Ohm resistance (R_{TONI}) between VIN and TON pins which can provide initial switching frequency and on-time for module. Besides, it also can connect additional resistor R_{TON} between VIN and TON pins to increase the switching frequency by paralleling.

VO PIN-13

The pin connects to output at load. It is also connected with internal drain of discharged MOSFET so that the output terminal can be discharged fleetly when power off.

VFB PIN-14

The VFB pin can be used to set the output voltage by the voltage divider network from the resistors RFB.

PGOOD PIN-15

The PGOOD pin is an open-drain output and a 10kOhm resistor is connected ADJ pin. If the 10kOhm pull-high resistor can not meet user's requirement, then user can use ADJ pin to do suitable adjustment for meeting requirement. Additionally, when the output voltage is 20% above or 10% below its set voltage, PGOOD pin gets polled low. It is held low until the output voltage returns to within these tolerances once more.

ADJ PIN-16

The relationship between ADJ pin and PGOOD pin is as Fig. 2. A typically resistance 10kOhm is integrated, the pin should be connected to +5V (or others power supply). User also can use the relationship between ADJ pin and PGOOD pin to adjust suitable pull resistance for meeting user's requirement.

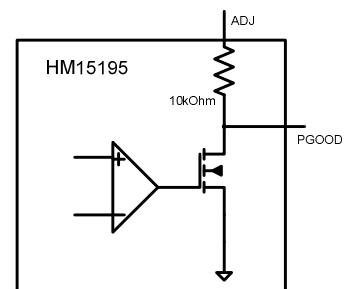


Fig. 2 The relationship between ADJ pin and PGOOD pin

APPLICATION INFORMATION

The typical HM15195 application circuit is shown as Fig 1. The switching frequency is increased by R_{TON} , the output voltage is determined by the resistor R_{FB} . Selection of resistor R_{SEN} can decrease initial over-current protection point. More detail description for application of HM15195 as below:

Programming the Output Voltage

The HM15195 has an internal 0.5V reference voltage. Output voltage can be programmed by the resistors R_{FB} . The computable equation is as below:

$$V_{OUT} = 0.5 \left(1 + \frac{10k}{R_{FB}} \right) \text{ (V)}$$

Note: 10k Ohm is integrated in module.

Increasing PWM Switching Frequency

HM15195 has an integrated frequency setting resistor 1M Ohm which switching frequency approximately is between 200kHz and 400kHz in different pairs of V_{IN} and V_{OUT} . Besides, user can determine R_{TON} to increase switching frequency for meeting requirement. It's computed equations as below:

For $0.5V < V_{OUT} < 3.3V$:

$$T_{ON} = 3.3 * 10^{-12} * (R_{TON} // 1M + 37 * 10^3) * \left(\frac{V_{OUT}}{V_{IN}} \right) + 50 * 10^{-9} \text{ (sec)}$$

Alternatively, for $3.3V < V_{OUT} < 5V$

$$T_{ON} = 0.85 * 3.3 * 10^{-12} * (R_{TON} // 1M + 37 * 10^3) * \left(\frac{V_{OUT}}{V_{IN}} \right) + 50 * 10^{-9} \text{ (sec)}$$

Where:

T_{ON} is on time

V_{OUT} is output voltage

V_{IN} is input voltage

R_{TON} is frequency setting resistor which located between V_{IN} pin and T_{ON} pin.

Next, using fundamental the relationship between the switching frequency f_{sw} and on time T_{ON} , the switching frequency can be found to meet requirement. Its calculated equations are as follows:

$$f_{SW} = \frac{V_{OUT}}{V_{IN} * T_{ON}} \text{ (Hz)}$$

Note: User does not need to design the resistor R_{TON} , because the integrated resistor has designed for optimum efficiency and output voltage ripple.

+5V Bias Supplies Connection

The HM15195 requires an external +5V bias supply in addition to system power. It supplies PWM controller and high / low side MOSFET gate driver. The +5V bias supply can be generated with an external linear or regulator or power supply devily. It can add an extra 2.2uF MLCC decoupling capacitor to enhancing the stability in $PVCC$ pin, but not necessary.

APPLICATION INFORMATION (CONTINUED)

Enable and Power Saving Mode (EN/PSV)

The EN/PSV pin enables the HM15195. When the EN/PSV is tied to +5V, the module and power saving mode are enabled. When the EN/PSV pin is tri-stated, this state will activate the module and the module will enter force CCM. If power saving mode is enabled, the power saving comparator will look for inductor current to cross zero whether is on eight consecutive switching cycles by comparing the PHASE node to PGND. Once observed, the module will enter power save mode and turn off low-side MOSFET when the current crosses zero. To improve light-load efficiency and add hysteresis, the on-time is increased by 50% in power saving mode for pulse skip. The efficiency improvement as light-loads more than offsets the disadvantage of slightly higher output ripple.

Power GOOD Output

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 20% above 10% below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. PGOOD is also held low during start-up and will not be allowed to transient high until soft start is over (440 switching cycles) and the output reaches 90% of its set voltage. There is a 5us delay built into the PGOOD circuitry to prevent false transitions.

Output Over-Voltage Protection

When the output exceeds 20% of its set voltage then the low-side MOSFET is latched on. That is discharging output energy to low side MOSFET which is in order to avoiding high voltage to damage the load. It stays latched on and the module is latched off until reset. There is a 5us delay built into the over voltage protection circuit to prevent false transitions.

Output Under-Voltage Protection

When the output voltage is 10% below its set voltage the output is latched in tri-stated condition. It stays latched and the module is latched off until reset. There is a 5us delay built into the under voltage protection circuit to prevent false transitions. Note: to reset from any fault, PVCC or EN/PSV must be toggled.

Over-Temperature

When an OTP fault is detected, the HM15195 over temperature protection circuit suspends PWM, but will not affect the PGOOD pin, or latch off the HM15195. The over temperature protection circuit measures the temperature of the silicon and activates when the rising threshold temperature TP_{OTPL} has been exceeded.

Power-On Reset, UV Lockout and Soft Start

An internal power-on reset (POR) occurs when PVCC exceeds 3V, starting up the internal biasing. PVCC under voltage lockout (UVLO) circuitry inhibits the module until PVCC rises above 4.2V. At this time the UVLO circuitry resets the fault latch and soft-start counter, and allows switching to occur if the device is enabled. Switching always starts with low-side switch signal to charge up the bootstrap capacitor. With the soft-start circuit (automatically) it will progressively limit the output current (by limiting the current out of the

APPLICATION INFORMATION (CONTINUED)

I_{SEN} pin) over a pre-determined time period of 440 switching cycles. The ramp occurs in four steps:

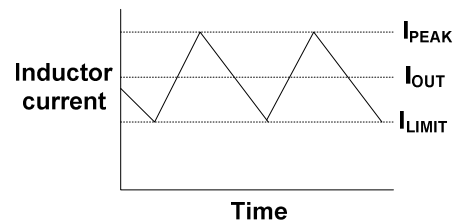
- (1) 110 cycles at 25% I_{SEN} with double minimum off-time (for purposes of the on-time one-shot, there is an internal positive offset of 120mV to V_{OUT} during this period to aid in startup).
- (2) 110 cycles at 50% I_{SEN} with normal minimum off time.
- (3) 110 cycles at 75% I_{SEN} with normal minimum off-time.
- (4) 110 cycles at 100% I_{SEN} with normal minimum off time.

At this point the output under-voltage and power good circuitry is enabled. There is 100mV of hysteresis built into the UVLO circuit and when PVCC falls to 4.1V (nom.) the output drivers are shut down and tri-stated.

Current Limit

Current limiting of the HM15195 can be accomplished by sensing voltage for on-state resistance of low-side MOSFET. R_{DS(ON)} sensing is more efficient and less expensive. R_{SEN} resistor between the I_{SEN} pin and PHASE pin sets the over current threshold. This resistor R_{SEN} is connected to a 10 μA current source within the module which is turned on when the low side MOSFET turns on. When the voltage drop across the low side MOSFET equals the voltage current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the low-side MOSFET falls below the voltage across the R_{SEN} resistor. In an extreme over-current situation, the top MOSFET will never turn back on and eventually the part will latch off due to output under-voltage (see Output Under-voltage Protection). The current sensing

circuit actually regulates the inductor valley current (see figure below). This means that if the current limit is set to 15A, the peak current through the inductor would be 15A plus the peak ripple current, and the average current through the inductor would be 15A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown below:



The equation for the current limit threshold is as follows:

$$I_{SEN} = 10 * 10^{-6} * \left(\frac{R_{SEN}}{R_{DS(ON)}} \right) A$$

The current limit looks at the “valley current” (I_{VALLEY}), which is average output current minus half the ripple current. The valley current is across the R_{SEN} resistor, positive

$$I_{VALLEY} = I_{OUT} - \left(\frac{I_{RIPPLE}}{2} \right) A$$

Where: I_{RIPPLE} is I_{PEAK} - I_{LIMIT}. Therefore, the current limit resistor (R_{SEN}) can be calculated by output current and valley current as

$$R_{SEN} = 1.4 * I_{VALLEY} * \left(\frac{R_{DS(ON)}}{10 * 10^{-6}} \right) Ohm$$

APPLICATION INFORMATION (CONTINUED)

Where :

R_{SEN} is equivalent resistance between PHASE and ISEN pins.

$R_{DS(ON)}$ is typically 7.2mOhm ($V_{gs}=4.5V$, $I_{DS}=30A$).

Note: HM15195 has integrated 20kOhm resistance (R_{SENI}). Therefore, the equivalent resistance of R_{SEN} is

$$R_{SEN} = \frac{R_{SENI} * \text{External } R_{SEN}}{R_{SENI} + \text{External } R_{SEN}} \text{ Ohms}$$

The current limit circuitry also protects against negative over-current (i.e. when the current is flowing from the load to PGND through the inductor and low-side MOSFET). In this case, when the low-side MOSFET is turned on, the PHASE node, (PHASE), will be higher than PGND initially. The HM15195 monitors the voltage at PHASE, and if it is greater than a set threshold voltage of 125mV (nom.) the low-side MOSFET is turned off. The device then waits for approximately 2.5 μ s and then LG goes high for 300ns (typ.), once more to sense the current. This repeats until either the over current condition goes away or the part latches off due to output over-voltage.

Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger capacitor, the less ripple expected but consider should be taken for the higher surge current during the power up. The HM15195 provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by the following formula :

$$C_{IN} = \frac{I_{IN} * \Delta t}{\Delta V}$$

Where :

C_{IN} is the input capacitance (μ F)

I_{IN} is the input current (A)

Δt is the turn on time of the high-side switch (μ s)

ΔV is the allowable peak to peak voltage (V)

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain terminal of the high side MOSFET and the source terminal of the low side MOSFET, in order to reduce the voltage ringing created by the switching current across parasitic circuit elements.

Output Capacitors

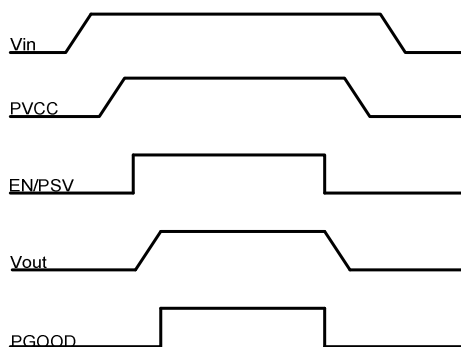
The HM15195 is designed for low output voltage ripple. The bulk output capacitors C_{OUT} is chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be low ESR tantalum capacitor, low ESR polymer capacitor and ceramic capacitors. The typical capacitance is 330 μ F, if all ceramic output capacitors are used. The internally optimized loop compensation provides sufficient stability margin for all ceramic capacitors applications. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required.

Thermal Consideration and Output Current De-rating

APPLICATION INFORMATION (CONTINUED)

Timing Chart

The timing chart can be helpful for engineers to see the operation of each pin of HM05125 and can be used to be the primary basis during the error detection. The timing chart of HM02125 during the normal operation is as follows:



When it comes to start-up, it should be noted that the internal mechanism of HM05125 does not allow the startup of PVCC to be faster than that of the input voltage, so in order to make it work normally, this problem should be avoided in applications.

PACKAGE DIMENSION

PACKAGE DESCRIPTION