

HM05125 High Efficiency DC/DC Module

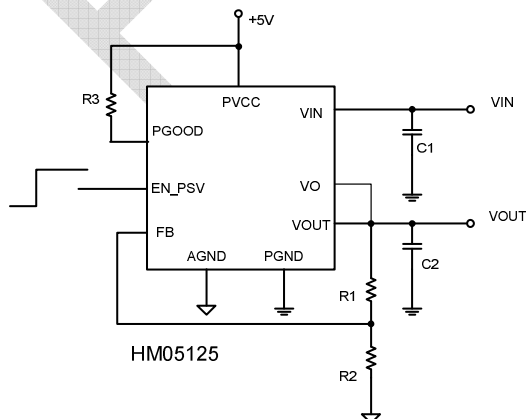
FEATURES

- Complete Switch Mode Power Supply
- Wide Input Voltage Range from +1.8V to 24V
- 5A DC Output Current
- Adjustable +0.5V to +5V Output Range
- Fast Transient Response
- Power Saving Mode Option
- Enable Function Option
- Power Good Indicator
- Internal Soft-Start
- Whole Protection Functions
- Pb-Free RoHS Compliant Package
- Small Footprint, Low Profile Surface Mount Hybrid Package (11mm×11mm×2.8mm)

APPLICATIONS

- Note Book Computers, UMPC
- I/O Supplies
- System Power Supplier
- Point of Load

TYPICAL SCHEMATIC



DESCRIPTION

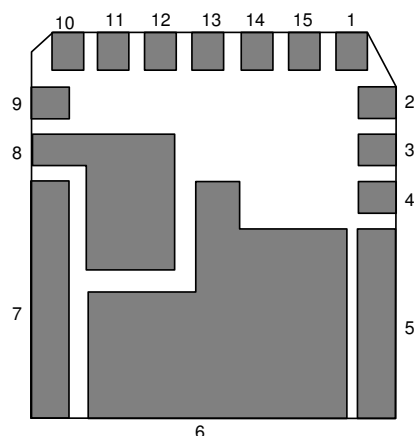
The HM05125 is a complete 5A, DC/DC step down power supply. Included in the package have the PWM controller, power MOSFETs, inductor, and most of support components. Operating over an input voltage range of 1.8V to 24V and supports an output voltage range of 0.5V to 5V that set by single dividing resistor. The high efficiency design delivers 5A continuous current. Only bulk input, output capacitors and few parameter setting components are needed to finish the design.

The HM05125 uses constant on-time control for fast transient response. The HM05125 has internal soft-start, current limit, over voltage protection, under voltage protection, power good output and soft discharge upon shutdown. The HM05125 can be configured to operate power saving mode (PSV) or not. At light loads, PSV enables the PWM controller to skip PWM pulses for better efficiency. The HM05125 has been set initial frequency and current limit for normally application which easy to design for power converter.

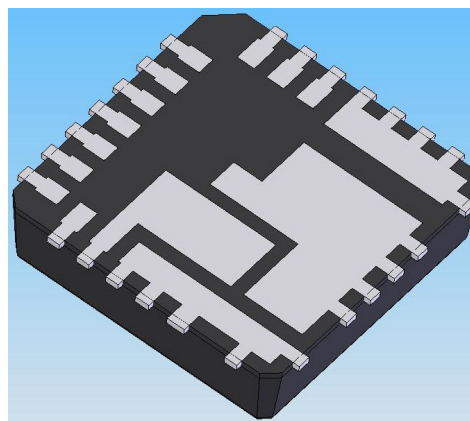
The low profile package (2.8mm) enables utilization of unused space on the bottom of PC boards for highly density point of load regulation. The HM05125 is packaged in a thermally enhanced, compact (11mm×11mm) and low profile (2.8mm) over-molded Hybrid Package Modular suitable for automated assembly by standard surface mount equipment. The HM05125 is Pb-free and RoHS compliance.

MODULE INFORMATION

Bottom View



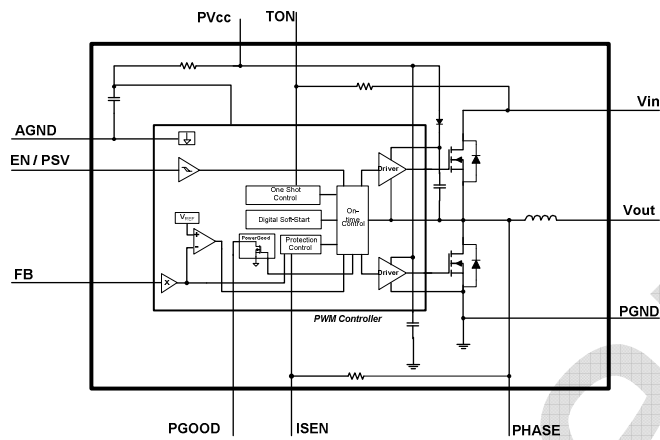
Physical View



Pin Definition:

Pin	Name	Description
1	VFB	Output voltage feedback input. Connect the resistor divider to adjust output.
2	VO	Connect to output for output discharge when module turned off.
3	VCC	5V power supply to PWM controller except gate drivers. Apply RC filter at this pin input. The RC filter is an option. User has no need to install.
4	PGND	Power ground
5	VOOUT	Connect to output
6	PHASE	High side MOSFET gate driver return
7	PGND	Power Ground
8	VIN	Connect to Input
9	PVCC	5V power supply for gate drivers. Connect 1uF or more between this pin and PGND to support instantaneous current for gate drivers. This capacitor is an optional component. User has no need to install.
10	ISEN	Setting over-current protection point. Connect resistor from this pin to PHASE to setting over-current threshold. User has no need to install, a 30kOhm is integrated.
11	AGND	Analog Ground
12	AGND	Analog Ground
13	PGOOD	Power-good signal output. Pull up to 5V with a pull-up resistor.
14	EN_PSV	Enable/Power save pin. Connect to ground to disable module. Connect to 3.3V or 5V to turn on module and activate power save mode. Float to turn on force CCM.
15	TON	On Time/Frequency adjustment. Connect to VIN. This resistor is an optional component, so it has not need to install.

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Limits	Unit
TON to AGND	-0.3 to +25	V
PVCC , EN / PSV, FB, PGOOD, Vo, ISEN to AGND	-0.3 to +6	V
PHASE to PGND	-1.2 to +30	V
T _c	100	°C
T _{stg}	-40 to +125	°C
TON to AGND	-0.3 to +25	V
VIN to PHASE	-1.2 to +30	V
PGND to AGND	-0.3 to +0.3	V

CAUTION : Stress over "Absolute Maximum Ratings" may cause permanent damage.

RECOMMENDED OPERATING RATINGS

Symbol	Parameter	Limits	Unit
VIN	Input supply voltage	1.8 to 24	V
VOUT	Output voltage	0.5 to 5.0	V
T _a	Ambient temperature range	-40 to 85	°C

Note: Over operating free-air temperature range.

ORDER INFORMATION

PART NUMBER	PACKAGE
HM05125	Hybrid Package (11mm × 11mm × 2.8mm)

THERMAL RESISTANCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Rth(j-a)	Thermal resistance from junction to ambient	Note 1	-	14.5	-	°C/W

Note 1 : Rth(j-a) is measured with the component mounted on a highly effective thermal conductivity test board on 0 LFM condition. The test board size is 114.3mm*101.5mm*1.6mm with 4 copper layers, and each copper trace thickness is 1 oz. The test condition is complied with JEDECE EIJ/JESD 51 Standards.

ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range, Vin = 19V / 12V, Vout = 1.5V, RTON=1MΩ

Input Capacitance=241μF, Output Capacitance=356μF, (Cyntec's EVM)

Input Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{Q(VIN)}	Input supply bias current	I _{out} = 0A V _{out} = 1.5V, Vin = 19V, EN/PSV = 5V Vin = 19V, EN/PSV = Tri-stated Vin = 12V, EN/PSV = 5V Vin = 12V, EN/PSV = Tri-stated		0.1 20 0.1 25		mA
I _{S(VIN)}	Input supply current	I _{out} = 5A, V _{out} = 1.5V, Vin = 19V Vin = 12V		0.52 0.8		A
Output Characteristics						
I _{OUT(DC)}	Load Rating		0	-	5	A
ΔV _{OUT} /ΔV _{IN}	Line regulation accuracy	EN/PSV = Tri-stated, Vin = 3.3V to 25V V _{out} = 1.5V, I _{out} = 0A V _{out} = 1.5V, I _{out} = 5A		0.1 0.1		%
ΔV _{OUT} /ΔI _{OUT}	Load regulation accuracy	EN/PSV = Tri-stated I _{out} = 0A to 5A V _{out} = 1.5V Vin = 19V, Vin = 12V,		1		%
V _{OUT(AC)}	Output ripple voltage*	EN/PSV = Tri-stated, I _{out} = 5A V _{out} = 1.5V, Vin = 19V, Vin = 12V		60		mVp-p

*Note: Output ripple voltage is dependent on ESR of output capacitors. For design of output capacitor ESR, please refer to HM05125 application note.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Over operating free-air temperature range, $V_{in} = 19V / 12V$, $V_{out} = 1.5V$, $R_{TON} = 1M\Omega$

Input Capacitance=241 μ F , Output Capacitance=356 μ F (Cyntec's EVM)

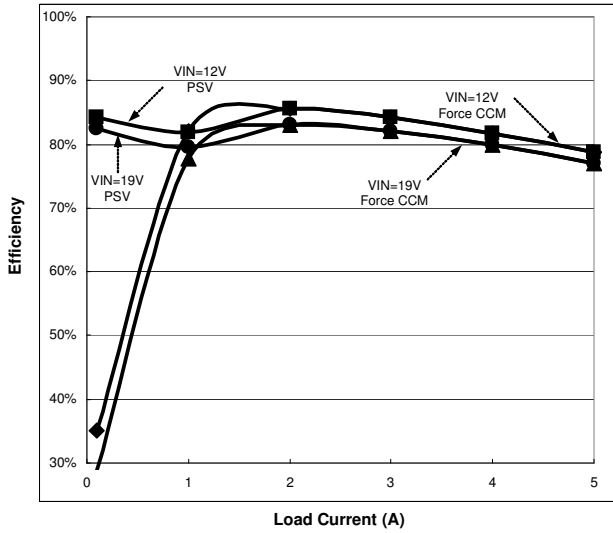
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Dynamic Characteristics						
ΔV_{OUT-DP}	Voltage change for positive load step	IOUT = 10% to 90% of 5A. Current slew rate = 2.5A/ μ S $V_{in} = 19V$, $V_{out} = 1.5V$ $V_{in} = 12V$, $V_{out} = 1.5V$	-	60	-	mVp-p
ΔV_{OUT-DN}	Voltage change for negative load step	IOUT = 90% to 10% of 5A. Current slew rate = 2.5A/ μ S $V_{in} = 19V$, $V_{out} = 1.5V$ $V_{in} = 12V$, $V_{out} = 1.5V$	-	60	-	mVp-p
Control Stage						
V_{FBTHR}	FB turn-on threshold	PVCC = 4.5V to 5.5V	0.494	0.5	0.506	V
R_{TONI}	Internal resistor between V_{in} and TON pins		0.99	1	1.01	M Ω
TON	PWM on-time	$V_{in} = 19V$, $V_{out} = 1.5V$, $I_{out} = 5A$ $R_{TONI} = 1M\Omega$ (Integrated)		300		nS
V_o	Output voltage range		-	0.5	PVCC	V
V_{ENLTHR}	EN low threshold voltage	EN/PSV low	-	1.2		V
V_{ENHTHR}	EN high threshold voltage	EN/PSV high	-	3.1		V
Fault Protection						
R_{SENI}	Internal resistor between ISEN and PHASE pins			30		k Ω
V_{UVF}	Output under voltage fault		-20	-10	-5	%
V_{OVF}	Output over voltage fault		+15	+20	+40	%
$PVCC_{UVTHR}$	PVCC under voltage threshold		3.7	4.0	4.3	V
TP_{OTPL}	Over temperature lockout		-	165	-	$^{\circ}$ C
PGOOD Stage						
V_{PGDLV}	PGOOD low output voltage	Sink 1mA	-	-	0.4	V
$V_{PGDUVTHR}$	PGOOD under voltage threshold		-12	-10	-8	%

TYPICAL PERFORMANCE CHARACTERISTICS

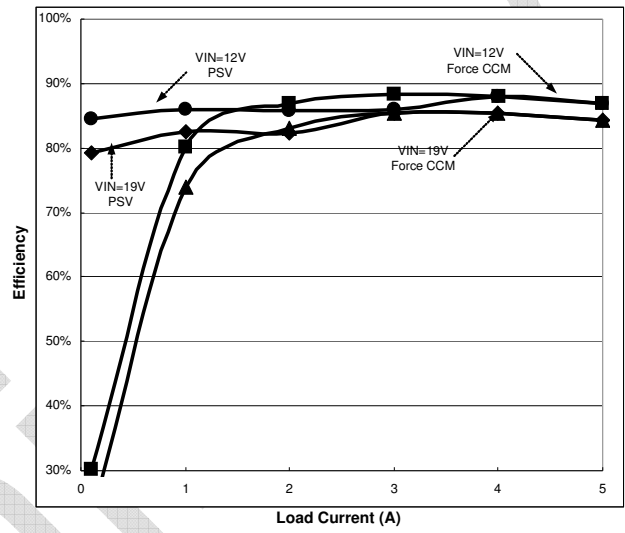
Efficiency Performance : Including Force CCM and Power Save Mode (PSV)

Test Condition: Room Temp., Input Capacitance=241uF, Output Capacitance=356uF (Cyntec's EVM)

Output Voltage=1.5V



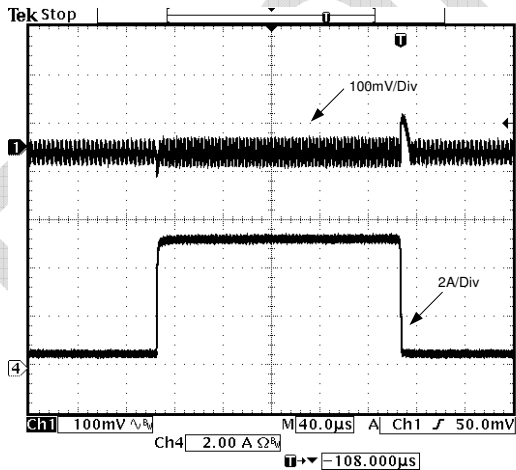
Output Voltage=3.3V



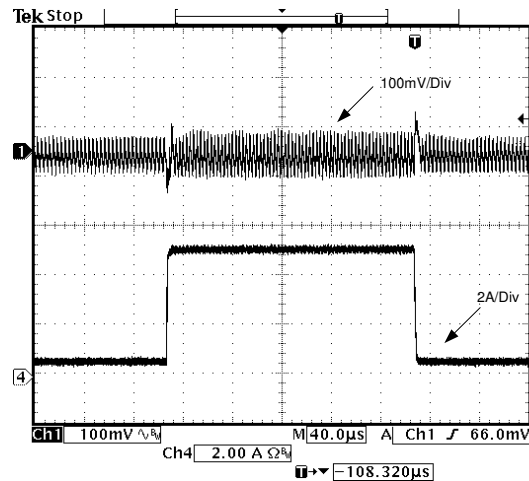
Load Transient Response Performance

Test Condition: Room Temp., Input Capacitance=241uF, Output Capacitance=356uF (Cyntec's EVM), Slew Rate=2.5A/us, Force Continuous Current Mode

Input Voltage=12V, Output Voltage=1.5V



Input Voltage=12V, Output Voltage=3.3V



TYPICAL APPLICATION CIRCUIT:

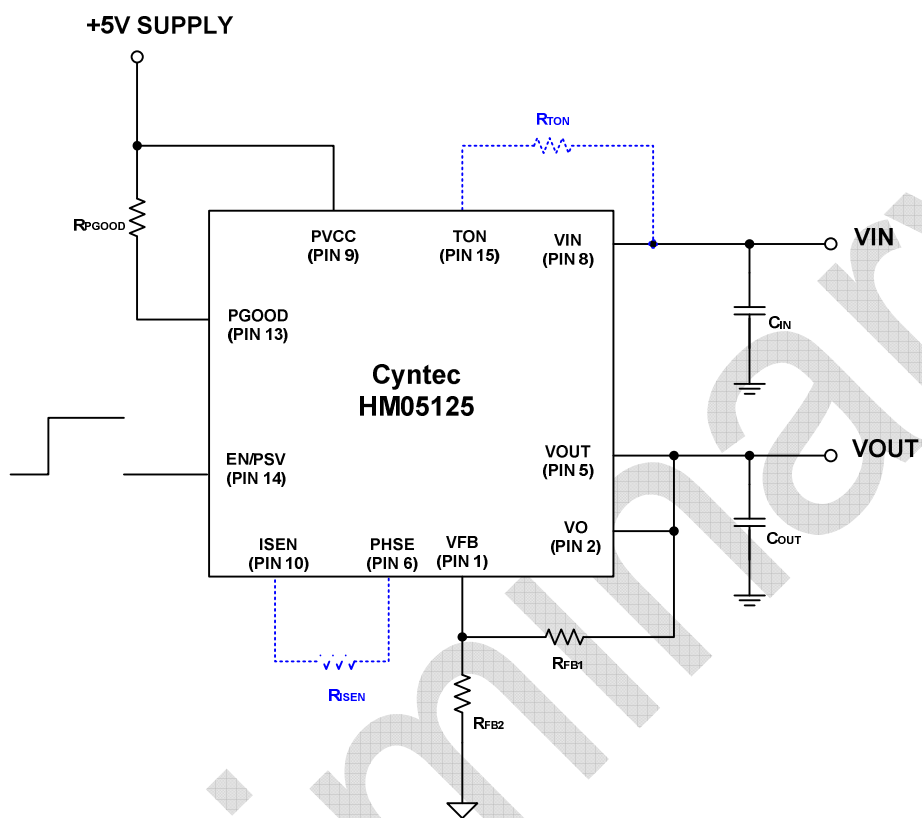


Fig. 1 Reference Circuit

Note: The blue dash lines represent these are options, user has no need to install.

PIN FUNCTIONS

FB PIN-1

The FB pin can be used to set the output voltage by the voltage divider network from resistors RFB1 and RFB2 (see Fig 1). The value of RFB1 is dependent on loop gain, its value recommended 10kOhm

VO PIN-2

The pin connects to output at load. It is also connected with internal drain of discharged MOSFET so that the output terminal can be discharged fleetly when power off.

VCC PIN-3

Supply voltage input for internal IC circuits except gate drivers. It can connect a capacitors to enhance filtering capability, but not necessary.

AGND PIN-11, PIN-12

The pin is the common of the HM05125. All signals should be referenced to AGND, NOT the PGND pin.
Note: signals like feedback signal of output, feedback terminal signal...etc.

VOOUT PIN-5

Power output pin. Apply output load between the pin and PGND. Recommend placing high frequency output decoupling capacitors between the pin and PGND as close as possible. Besides, connect to top resistor RFB1 of the voltage divider network to set output voltage.

PHASE PIN-6

The PHASE pin is the switching node between high and low side MOSFET. It also returns the current path for the high side MOSFET driver. And detecting the low-side MOSFET drain voltage for the over current limits point. Besides, for good thermal performance, the node needs wide but "smart".

PGND PIN-4, PIN-7

Power ground pin for both input and output return path. It needs to connect one (or more) ground plan immediately which is recommended to minimize the effect of switching noise and copper losses, and maximize heat dissipation.

VIN PIN-8

Power input pin. Apply input voltage between the pin and PGND pin. Recommend placing input capacitors directly between VIN pin and PGND pin. Besides, the input capacitors should place to module as close as possible.

PVCC PIN-9

The PVCC pin is the supply voltage for gate drivers. This +5V bias supply can be generated by linear or series pass regulator.

PIN FUNCTIONS (CONTINUED)

ISEN PIN-10

The ISEN pin is the input for the over current protection (OCP) setting. Which compares $R_{ds(on)}$ of low-side MOSFET to set the threshold. The HM05125 has an initial threshold, hence use doesn't need to design the threshold if this threshold value meets user's requirement. The threshold can be refereed by Application Note of HM05125. Beside, it also can connect additional resistor between PHASE pin and ISEN pin to increase the threshold.

PGOOD PIN-13

The PGOOD pin is an open-drain output and requires a pull-up resistor. When the output voltage is 20% above or 10% below its set voltage, PGOOD pin gets polled low. It is held low until the output voltage returns to within these tolerances once more.

EN_PSV PIN-14

The EN / PSV pin enables the supply. When EN / PSV is tied to PVCC, the HM05125 is enabled and power save will able be enabled. When the EN / PSV pin is tri-stated, an internal pull-up will activate the HM05125 and power save will be disabled.

TON PIN-15

The TON pin programs the PWM switching frequency due to it can determine the high-side switch turn-on time. The HM05125 has initial set this parameter to approach integrated completely. It is included internal 1M Ohm resistance (R_{TONI}) between VIN and TON pins which can provide initial switching frequency and on-time for module. Besides, it also can connect additional resistor R_{TON} between VIN and TON pins to increase the switching frequency by paralleling.

APPLICATION INFORMATION

The typical HM05125 application circuit is shown as Fig 1. The switching frequency is increased by R_{TON} , the output voltage is determined by the voltage-divider network R_{FB1} and R_{FB2} . Selection of resistor R_{SEN} can change over-current protection point. More detail description for application of HM05125 as below:

Programming the Output Voltage

The HM05125 has an internal 0.5V reference voltage. Output voltage can be programmed by the dividing resistors R_{FB1} and R_{FB2} .

$$V_{OUT} = 0.5 \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \text{ (V)}$$

Note that the recommended R_{FB1} value is 10kOhm.

Increasing PWM Switching Frequency

HM05125 has an integrated frequency setting resistor 1MOhm which switching frequency approximately is between 200kHz and 300kHz in different pairs of VIN and VOUT. Besides, user can determine R_{TON} to increase switching frequency for meeting requirement.

It's computed equations as below:

For $0.5V < V_{OUT} < 3.3V$:

APPLICATION INFORMATION (CONTINUED)

$$T_{ON} = 3.3 * 10^{-12} * (R_{TON} // 1M + 37 * 10^3) * \left(\frac{V_{OUT}}{V_{IN}}\right) + 50 * 10^{-9} \text{ (sec)}$$

Alternatively, for $3.3V < V_{OUT} < 5V$

$$T_{ON} = 0.85 * 3.3 * 10^{-12} * (R_{TON} // 1M + 37 * 10^3) * \left(\frac{V_{OUT}}{V_{IN}}\right) + 50 * 10^{-9} \text{ (sec)}$$

Where

T_{ON} is on time

V_{OUT} is output voltage

V_{IN} is input voltage

R_{TON} is frequency setting resistor which located between V_{IN} pin and T_{ON} pin.

Next, using fundamental the relationship between the switching frequency f_{SW} and on time T_{ON} , the switching frequency can be found to meet requirement. Its calculated equations are as follows:

$$f_{SW} = \frac{V_{OUT}}{V_{IN} * T_{ON}} \text{ (Hz)}$$

Note: User does not need to design the resistor R_{ton} , because the integrated resistor has designed for optimum efficiency and output voltage ripple.

+5V Bias Supplies Connection

The HM05125 requires an external +5V bias supply in addition to system power. It supplies PWM controller and high / low side MOSFET gate driver. The +5V bias supply can be generated with an external linear or regulator or power supply devilry. It can add an extra 2.2uF MLCC decoupling capacitor to enhancing the stability in

PVCC pin, but not necessary.

Enable and Power Saving Mode (EN/PSV)

The EN/PSV pin enables the HM05125. When the EN/PSV is tied to +5V, the module and power saving mode are enabled. When the EN/PSV pin is tri-stated, this state will activate the module and the module will enter force CCM. If power saving mode is enabled, the power saving comparator will look for inductor current to cross zero whether is on eight consecutive switching cycles by comparing the PHASE node to PGND. Once observed, the module will enter power save mode and turn off low-side MOSFET when the current crosses zero. To improve light-load efficiency and add hysteric, the on-time is increased by 50% in power saving mode for pulse skip. The efficiency improvement as light-loads more than offsets the disadvantage of slightly higher output ripple.

Power GOOD Output

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 20% above 10% below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. PGOOD is also held low during start-up and will not be allowed to transient high until soft start is over

APPLICATION INFORMATION (CONTINUED)

(440 switching cycles) and the output reaches 90% of its set voltage. There is a 5 μ s delay built into the PGOOD circuitry to prevent false transitions.

Output Over-Voltage Protection

When the output exceeds 20% of its set voltage then the low-side MOSFET is latched on. That is discharging output energy to low side MOSFET which is in order to avoiding high voltage to damage the load. It stays latched on and the module is latched off until reset. There is a 5 μ s delay built into the over voltage protection circuit to prevent false transitions.

Output Under-Voltage Protection

When the output voltage is 10% below its set voltage the output is latched in tri-stated condition. It stays latched and the module is latched off until reset. There is a 5 μ s delay built into the under voltage protection circuit to prevent false transitions. Note: to reset from any fault, PVCC or EN/PSV must be toggled.

Over-Temperature

When an OTP fault is detected, the HM05125 over temperature protection circuit suspends PWM, but will not affect the PGOOD pin, or latch off the HM05125. The over temperature protection circuit measures the temperature of the silicon and activates when the rising threshold temperature TP_{OTPL} has been exceeded.

Power-On Reset, UV Lockout and Soft Start

An internal power-on reset (POR) occurs when PVCC exceeds 3V, starting up the internal biasing. PVCC under voltage lockout (UVLO) circuitry

inhibits the module until PVCC rises above 4.2V. At this time the UVLO circuitry resets the fault latch and soft-start counter, and allows switching to occur if the device is enabled. Switching always starts with low-side switch signal to charge up the bootstrap capacitor. With the soft-start circuit (automatically) it will progressively limit the output current (by limiting the current out of the ISEN pin) over a predetermined time period of 440 switching cycles.

The ramp occurs in four steps:

- (1) 110 cycles at 25% ISEN with double minimum off-time (for purposes of the on-time one-shot, there is an internal positive offset of 120mV to VOUT during this period to aid in startup).
- (2) 110 cycles at 50% ISEN with normal minimum off time.
- (3) 110 cycles at 75% ISEN with normal minimum off-time.
- (4) 110 cycles at 100% ISEN with normal minimum off time.

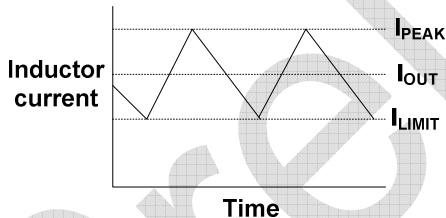
At this point the output under-voltage and power good circuitry is enabled. There is 100mV of hysteresis built into the UVLO circuit and when PVCC falls to 4.1V (nom.) the output drivers are shut down and tri-stated.

Current Limit

Current limiting of the HM05125 can be accomplished by sensing voltage for on-state resistance of low-side MOSFET. R_{DS(ON)} sensing is more efficient and less expensive. R_{SEN} resistor between the ISEN pin and PHASE pin sets the over current threshold. This resistor R_{SEN} is connected to a 10 μ A current source within the module which is turned on when the low side MOSFET turns on.

APPLICATION INFORMATION (CONTINUED)

When the voltage drop across the low side MOSFET equals the voltage current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the low-side MOSFET falls below the voltage across the R_{SEN} resistor. In an extreme over-current situation, the top MOSFET will never turn back on and eventually the part will latch off due to output under-voltage (see Output Under-voltage Protection). The current sensing circuit actually regulates the inductor valley current (see figure below). This means that if the current limit is set to 5A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 5A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown below:



The equation for the current limit threshold is as follows:

$$I_{SEN} = 10 * 10^{-6} * \left(\frac{R_{SEN}}{R_{DS(ON)}} \right) A$$

The current limit looks at the “valley current” (I_{VALLEY}), which is average output current minus half the ripple current. The valley current is across the R_{SEN} resistor, positive

$$I_{VALLEY} = I_{OUT} - \left(\frac{I_{RIPPLE}}{2} \right) A$$

Where: I_{RIPPLE} is $I_{PEAK} - I_{LIMIT}$. Therefore, the current limit resistor (R_{SEN}) can be calculated by output current and valley current as

$$R_{SEN} = 1.4 * I_{VALLEY} * \left(\frac{R_{DS(ON)}}{10 * 10^{-6}} \right) Ohm$$

Where :

R_{SEN} is equivalent resistance between PHASE and ISEN pins.

$R_{DS(ON)}$ is typically 26mOhm ($V_{GS}=4.5V$, $I_{DS}=7A$).

Note: HM05125 has integrated 30kOhm resistance (R_{SENI}). Therefore, the equivalent resistance of R_{SEN} is

$$R_{SEN} = \frac{R_{SENI} * External R_{SEN}}{R_{SENI} + External R_{SEN}} Ohms$$

The current limit circuitry also protects against negative over-current (i.e. when the current is flowing from the load to PGND through the inductor and low-side MOSFET). In this case, when the low-side MOSFET is turned on, the PHASE node, (PHASE), will be higher than PGND initially. The HM05125 monitors the voltage at PHASE, and if it is greater than a set threshold voltage of 125mV (nom.) the low-side MOSFET is turned off. The device then waits for approximately 2.5 μs and then LG goes high for 300ns (typ.), once more to sense the current. This repeats until either the over current condition goes away or the part latches off due to output over-voltage.

APPLICATION INFORMATION (CONTINUED)

Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger capacitor, the less ripple expected but consider should be taken for the higher surge current during the power up. The HM05125 provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by the following formula :

$$C_{IN} = \frac{I_{IN} \times \Delta t}{\Delta V}$$

Where :

C_{IN} is the input capacitance (uF)

I_{IN} is the input current (A)

Δt is the turn on time of the high-side switch (us)

ΔV is the allowable peak to peak voltage (V)

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain terminal of the high side MOSFET and the source terminal of the low side MOSFET, in order to reduce the voltage ringing created by the switching current across parasitic circuit elements.

Output Capacitors

The HM05125 is designed for low output voltage ripple. The bulk output capacitors C_{OUT} is chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be low ESR tantalum capacitor, low ESR polymer capacitor and ceramic capacitors. The typical capacitance is 330uF, if all ceramic output capacitors are used. The

internally optimized loop compensation provides sufficient stability margin for all ceramic capacitors applications. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required.

Thermal Consideration and Output Current De-rating

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 114.5mm*101.5mm*1.6mm with 4 copper layers, and each copper trace thickness is 1 oz. The case temperature of module sensing point is shown as Fig 2. Then $R_{th(j-a)}$ and $R_{th(j-c)}$ are measured with the component mounted on a highly effective thermal conductivity test board on 0 LFM condition.

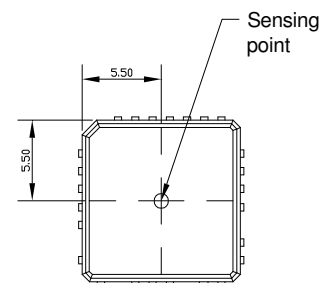


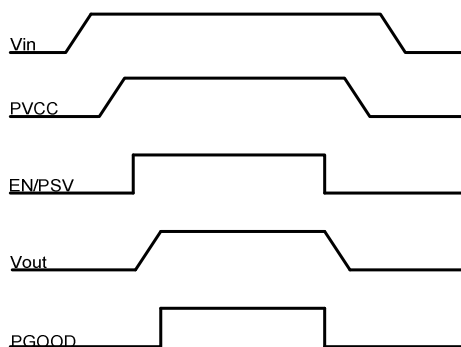
Fig 2. Case Temperature Sensing Point (Top view)

The HM05125 module is packaged in 11x11x2.8mm QFN packages that are constructed with copper lead frames that have exposed thermal pads. The output ability is function of input voltage/current, output voltage/current and ambient temperature factor etc.. For long-term reliability, HM05125 module is designed for using when the case temperature is below 100°C for long term operating consideration. Although the limitation of junction temperature of semiconductor devices is up to 150°C.

APPLICATION INFORMATION (CONTINUED)

Timing Chart

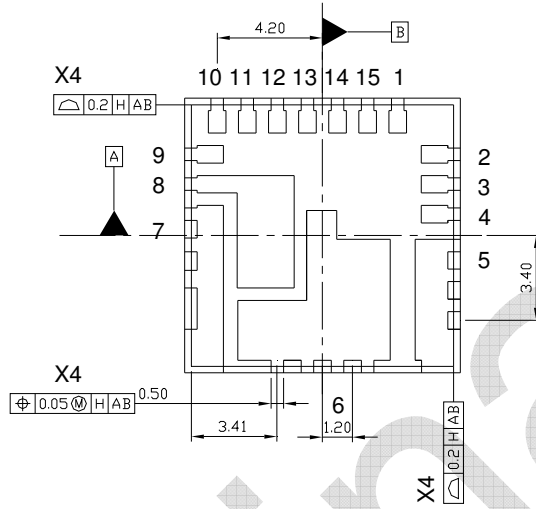
The timing chart can be helpful for engineers to see the operation of each pin of HM05125 and can be used to be the primary basis during the error detection. The timing chart of HM02125 during the normal operation is as follows:



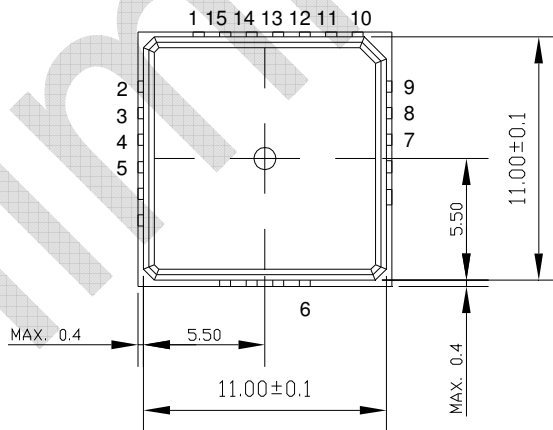
When it comes to start-up, it should be noted that the internal mechanism of HM05125 does not allow the startup of $PVCC$ to be faster than that of the input voltage, so in order to make it work normally, this problem should be avoided in applications.

PACKAGE DIMENSION

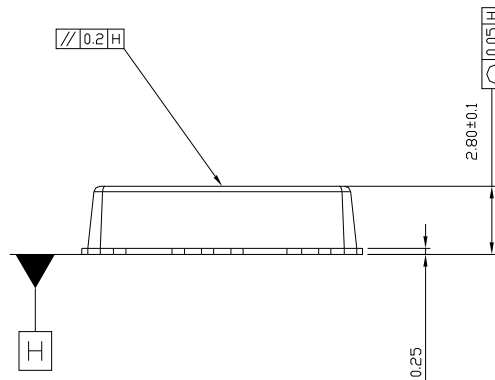
Bottom View:



Top View:



Side View:



PACKAGE DESCRIPTION

Introduction

The structure of HM05125 belongs to Quat-Flat pack-No leads package (QFN). This kind of package has some advantages like good thermal and electrical conductivity, low weight, small size, etc. As QFN structure is suitable for surface mounting technology, more and more uses in industry are concerned recently.

This reference shows the PCB layout pattern design, stencil pattern design and reflow profile parameters. It is noted that these guidelines are general design rules. Users could modify parameters according to their real application.

HM05125 contains several types of devices. There are resistor, capacitor, inductor, MOSFETs and control IC. The bottom of HM05125 is lead-frame footprint that transmits electrons and heat effectively. And polymer compound is covered and formed on the module to protect these devices. The module has a small size of 11x11x2.8 mm.

(Fig 1, Fig 2, Fig 3)

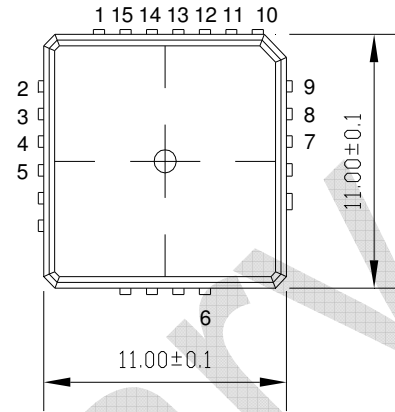


Fig. Top View

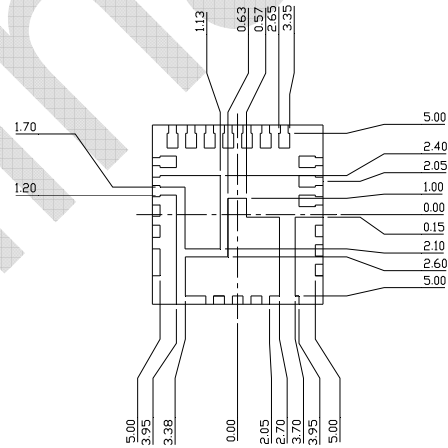


Fig 2. Bottom View

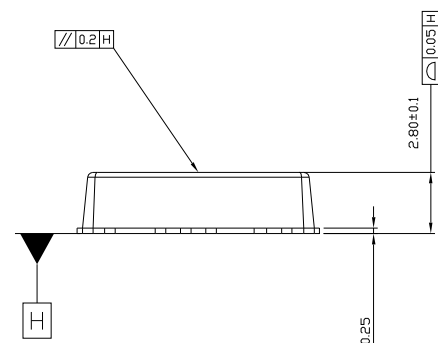


Fig 3. Side View

PACKAGE DESCRIPTION (CONTINUED)

PCB Layout Pattern Design

The bottom of HM05125 is lead-frame footprint, which could be attached to PCB by surface mounting process. Fig 4 shows the PCB layout pattern. The PCB layout pattern has an extended distance of 1.3mm toward outside. But the distance between PCB pads is still kept in 1mm, the same as lead-frame design. This idea is to help soldering more completely. It is suggested that user designs smaller PCB layout pattern with corresponding HM05125 to avoid forming short circuit when soldering. However, the reduction percentage of each pad area of the PCB layout pattern is not equal. Large pads of the pattern are usually reduced more area and small pads have less reduction.

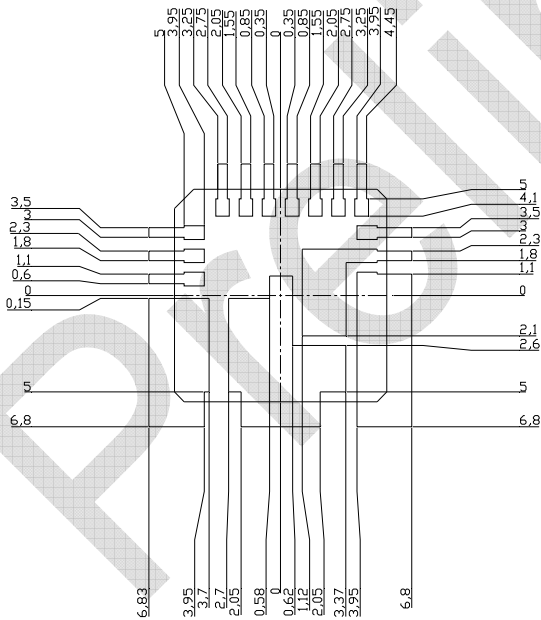


Fig. 4 Recommended PCB Layout Pattern

Stencil Pattern Design

Solder-printing method is very popular in surface mounting process. The stencil pattern design affects soldering very much. Fig 5 is an example of stencil pattern, which Fig 5 uses square pads. No matter circle or square pads, they have similar design rules. The gap width between pad to pad is 0.6mm. User should consider the symmetry of the whole stencil pattern when designing its pads. Designing larger pads for the stencil pattern would be a better choice. It is recommended that the stencil printing area should be 55% to 75% coverage of the total PCB layout pattern. 0.1mm thickness of stencil is also recommended for the use of printing so that the solder thickness could reach about 120 μ m, a proper solder thickness.

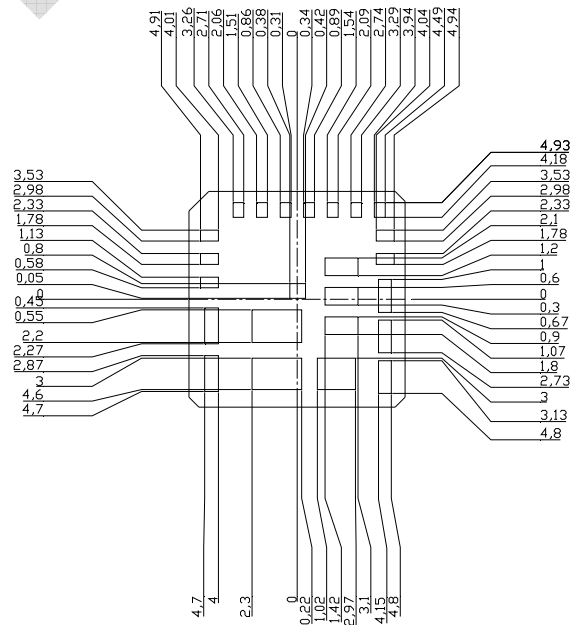


Fig. 5 Stencil Pattern with Square Pads

PACKAGE DESCRIPTION (CONTINUED)

Reflow Parameters

Lead-free soldering process is a standard of making electronic products. Many solder alloys like Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi and so on are used extensively to replace traditional Sn/Pb alloy. Here the Sn/Ag/Cu alloy (SAC) are recommended for process. In the SAC alloy series, SAC305 is a very popular solder alloy which contains 3% Ag and 0.5% Cu. It is easy to get it. Fig. 6 shows an example of reflow profile diagram. Typically, the profile has three stages. During the initial stage from 70°C to 90°C, the ramp rate of temperature should be not more

than 1.5°C/sec. The soak zone then occurs from 100 to 180°C and should last for 90 to 120 seconds. Finally the temperature raises to 230 °C ~245°C and cover 220°C in 30 seconds to melt the solder. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and user could switch to optimize the profile according to various solder type and various manufactures' formula.

Recommended Reflow Profile
OL213 Solder Paste: SAC305(Sn96.5/Ag3.0/Cu0.5) Alloy, mp. 216~219°C

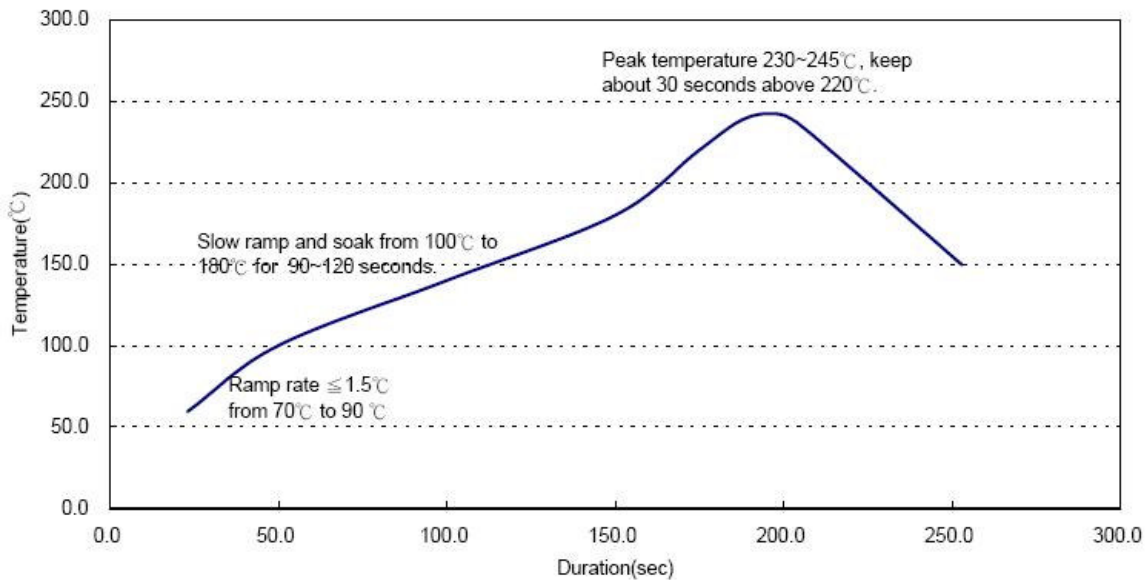


Fig. 6 Recommended Reflow Profile